<u>APPLICATION NOTE:</u>

New Techniques for Testing Power Factor Correction Circuits

Abstract:

This paper describes how to test the feedback loops in power factor correction (PFC) chips for stability. It discusses measurement techniques, stability guidelines, and loop bandwidth considerations for a range of manufacturers and integrated circuits (ICs), with emphasis on the new ICs developed recently. Stability testing is important because loop bandwidth and stability affect how fast the circuit will respond to source voltage transients and load changes. Power factor correction circuits often have two feedback loops. Both loops can have stability problems, and both loops can be tested for stability. One is a relatively slow loop that senses and sets the average output voltage. The other is a relatively fast loop that senses the instantaneous AC input voltage and tries to make the AC input current proportional to it. This second loop has a dynamically changing operating point and presents special measurement challenges. This paper describes procedures for testing both loops and gives guidelines and examples for …several chips.

Introduction

Power factor correction is being increasingly required as a feature of new power supply designs. Power factor correction takes the form of a new "front end" of power supplies, adding circuitry to shape the input current into an image of the input voltage and therefore making the power supply input look resistive to the source, usually the AC mains. One power supply vendor told us recently "every new specification I receive requires power factor correction, even at power levels as low as 200 watts."

The impetus for this requirement is new regulations, both in the U.S.A. and Europe, limiting the harmonic content of the input current of electrical equipment. This requirement has good and bad side effects. The good, of course, is that electrical power waveforms around the world will be cleaned up considerably when enough time has passed for these new units to supplant older designs now in the field. The bad is that the efficiency of power supplies is reduced, due to the double conversion required, and the size, weight, complexity, and cost of new designs inevitably will increase to accommodate the new feature.

In addition to the new circuitry, one or two additional feedback loops are required to control at least the output voltage of the new circuitry, and usually the input current waveform as well. The bandwidth of the voltage loop is critical since if it is too slow the system will not have a timely response to transients, and if too fast, it will distort the input current waveform and destroy the very reason the circuitry was added in the first place. The current loop, if there is one, also has critical bandwidth and

stability criteria and moreover is very difficult to measure since the operating point of the circuit is constantly changing as the line voltage changes. Venable Industries is a company dedicated to testing and optimizing feedback loops, hence our interest in this subject.

Overview

There are four, or perhaps five, approaches to implementation of power factor correction circuits. These are:

Discontinuous Flyback (constant frequency) Continuous Boost-average current sensing (usually constant frequency)

Continuous Boost-peak current sensing (usually constant frequency)

Boost-peak current sensing with current reset to zero each cycle (variable frequency)

Continuous Boost-hysteretic current sensing (variable frequency). This is a special chip made only by Cherry Semiconductor that controls both the peak and valley of the inductor current.

Discontinuous Flyback

The discontinuous flyback, shown in Figure 1, is the simplest of all the PFC circuits. It operates on the principle that discontinuous flyback converters, operated at fixed duty cycle and fixed frequency, draw current from the line directly proportional to the input voltage with no feedback or other special measures required to make this happen. In this special case there is only one feedback loop, the one to regulate output voltage. This is done by sensing the output voltage, comparing it to a reference in an op amp, and using the op amp output to control the duty cycle of the pulse width modulator (PWM). The disadvantages of this approach are that the peak current and voltage on the power transistor are much higher than with other approaches and that considerable filtering is required to smooth the current pulses into a sine wave.
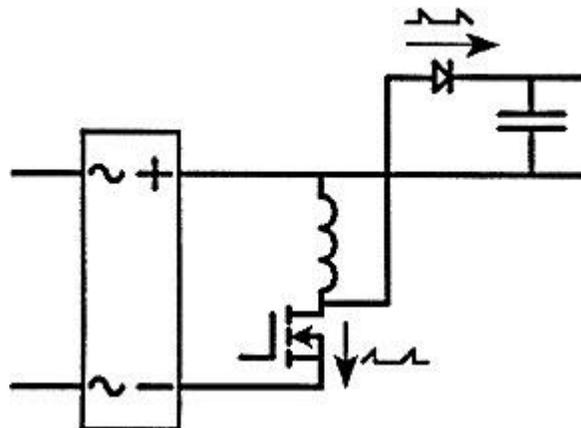

Figure 1. Discontinuous flyback PFC circuit

Continuous Boost with Average Current Sensing

Most PFC circuits use the boost converter topology. Figure 2 shows a boost converter with average current sensing. The current sense resistor is placed in the DC return leg opposite the energy storage inductor. The advantages of this boost topology are that the input is a relatively smooth waveform and therefore easy to filter, and that there is a convenient place to sense current (as shown) so that the current can be controlled to match the input voltage waveform. This approach (and all the other boost converters) has two feedback loops. One is a fast loop that controls the instantaneous input current to have the same shape as (make it proportional to) the instantaneous input voltage. The other loop is a slow loop that adjusts the overall amplitude of the input current (and therefore the output current) to keep the output voltage constant. As before, the performance of each of these loops is critical to achieving the goal of low power factor. Fortunately, most loops can be tested in a straightforward manner using standard Venable techniques.
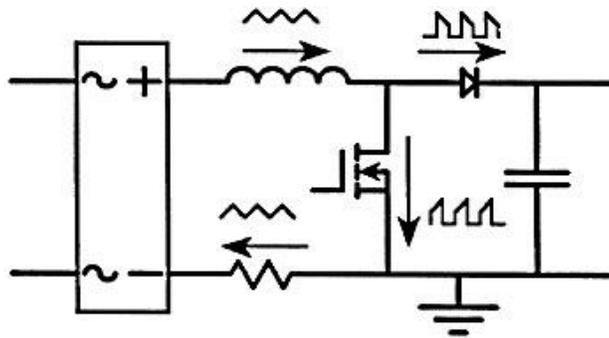

Figure 2. Continuous boost with average current sensing

This particular implementation, average current sensing, should give the best overall performance if implemented correctly because the variable being sensed (instantaneous input current) is exactly the one that needs to be controlled. The difficulty comes from the fact that the instantaneous input voltage is a rectified sine wave and is changing from zero to the peak value and back to zero 100 or 120 times per second, and this is the reference signal the current has to track. (This difficulty is shared by all boost topologies.)

Continuous Boost with Peak Current Sensing

A power supply control approach that has become popular in recent years is that of current mode control. In this approach, the peak transistor current is the directly controlled variable rather than duty cycle as in the previous approach. This is not as accurate as the average current approach since the controlled variable (peak current) is not exactly equal to the desired variable (average current), but since the peak-to-peak inductor ripple is relatively small (typically 10% of the DC value) the error introduced is not large and reasonable power factor can be achieved with this approach.

Figure 3 shows a boost converter with peak current sensing. The current sense resistor is series with the source of the power FET. Transistor current is initiated by the PWM clock and terminated when the transistor current reaches a peak level proportional to the instantaneous value of input voltage. Since PFC boost converters operate at a duty cycle greater than 50% for at least a portion of the input waveform, slope compensation must be incorporated to prevent open loop oscillation of the current mode control loop. Most current mode PFC ICs have provision for slope compensation.
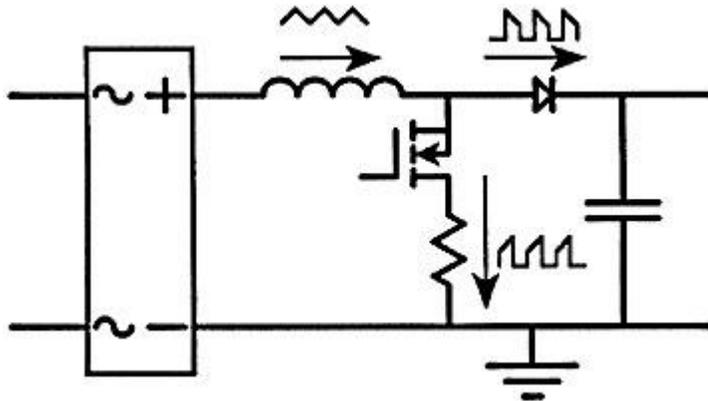
Figure 3. Continuous boost with peak current sensing

As in the other boost topologies, there are two feedback loops. One, the slow loop which controls the constant of proportionality between input voltage and input current, is the same as before with the requirement of a tightly controlled bandwidth to prevent both slow response to transients and distortion of the current waveform. It is essential to measure this bandwidth at least on a sample basis, if not on every production unit. The performance will vary from chip-to-chip and vary significantly from lot-to-lot, especially if chips from more than one manufacturer are used interchangeably.

The other, the fast current loop which controls input current, presents special measurement problems but is also essential to measure because of the possibility of oscillation due to current mode control operated at greater than 50% duty cycle. It is not possible to measure the open loop gain of the current loop directly because it is essentially digital. It is easy, however, to measure the closed loop gain. The closed loop gain is the transfer function from reference input (usually the output of an internal multiplier) to the input current, which is the energy storage inductor current and can be measured with a current probe on one of the inductor leads. The stability of the open loop gain can inferred from this closed loop measurement. Figures 4 and 5 show typical closed loop transfer functions for circuits with open loop bandwidth of 3.16 kHz and phase margins of 72° and 20° respectively.
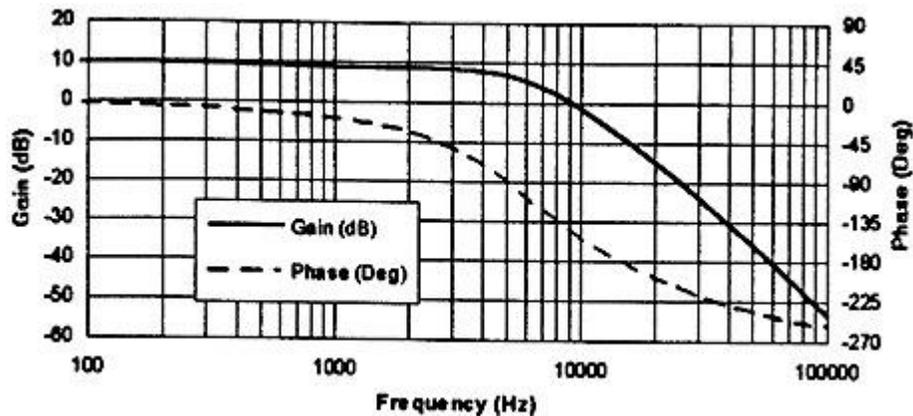

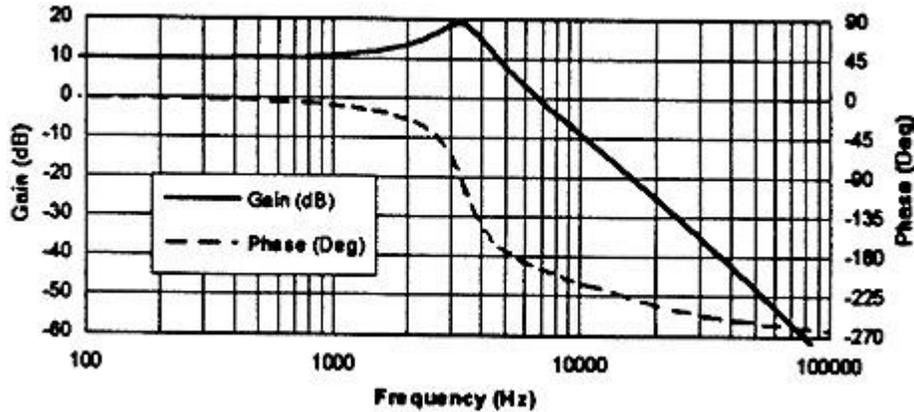*Figure 4. Closed loop with 72° open loop*

Figure 5. Closed loop with 20° open loop

There will be more and more peaking in the closed loop transfer function as the phase margin of the open loop transfer function is reduced. Phase margin of current mode control loops is adjusted by the amount of slope compensation provided. The open loop gain can also be calculated from closed loop data with proper software tools.

Boost with Current Reset to Zero

Another control approach with boost converters looks like current mode control, but incorporates additional circuitry to sense when the inductor current declines to zero in the off portion of the power transistor cycle. At that point the transistor is triggered on again, rather than from a PWM clock as in conventional current mode control. The net result of this arrangement is a waveform that always starts from zero, reaches a peak equal to twice the average for that instant of time, and then declines to zero again. Figure 6 shows a schematic with typical waveforms. The advantages of this approach are:

Since the current waveform is a triangle wave with zero current as a base, the controlled variable (peak current) is theoretically exactly twice the average current, so the performance of the power factor control aspect of the circuit should approach that of the average current mode control scheme. Because the current is constrained to a fixed value (zero) at one point in every cycle, one degree of freedom is removed from the state equations and slope compensation is not required to make the circuit openloop stable. The energy storage inductor is relatively small. Transistor turn-on losses are eliminated.

The Disadvantages Are:

The peak current in the transistor is almost twice that of other boost schemes. Transistor turn-off losses are at least doubled Extra filtering is required to smooth the large AC waveform drawn by this approach.

As can be seen from the above advantages and disadvantages listing, no one approach is perfect and engineers can rest assured that their judgment will still be needed to select from the many approaches available.
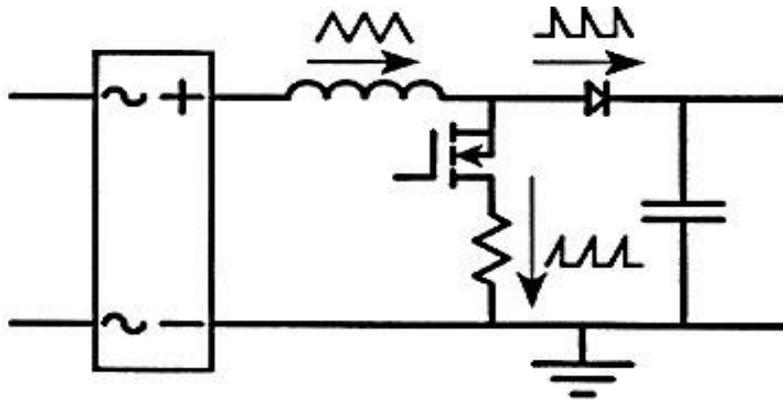
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Figure 6. Boost with peak current sensing -- current resets to zero each cycle

Boost with Hysteretic Control

A special case of the above approach is one invented some years ago by Cherry Semiconductor where both the peak and valley of the current waveform are controlled. Cherry calls this Hysteretic Control. This approach also removes a degree of freedom from the circuit and removes the need for slope compensation. Since the difference between the controlled variable (peak current) and the average current is known and programmable, accurate power factor control is also achievable. The AC ripple on the inductor can also be controlled, usually to the same general range (10% of DC) that the other boost PFC circuits use.

Table 1. Selection of Power Factor Correction ICs and Manufacturers

Manufacturer	Part Number	Topology		PWM	Method				Frequency	
		Boost	Flyback	Additional PWM	Average current sensing	Peak current sensing with slope comp.	Zero current sensing	Hysteretic current sense	Fixed	Variable
Cherry Semiconductor	CS3810	x	x					x		x
Linear Technology	LT1248	x			x				x	
Linear Technology	LT1249	x			x				x	
Linfinity Microelectronics	SG3561A	x					x			x
Linfinity Microelectronics	LX1562,1563	x					x			x
Micro Linear	ML4812	x				x			x	
Micro Linear	ML4813		x						x	
Micro Linear	ML4819	x		x		x			x	
Micro Linear	ML4821	x			x				x	

Table 1. Selection of Power Factor Correction ICs and Manufacturers

Manufacturer	Part Number	Topology		PWM	Method				Frequency	
		Boost	Flyback	Additional PWM	Average current sensing	Peak current sensing with slope comp.	Zero current sensing	Hysteretic current sense	Fixed	Variable
Motorola	MC34261	x					x			x
Motorola	MC34262	x					x			x
SGS-Thomson	L4981 A/B	x			x				x	
SGS-Thomson	L6560	x					x			x
Siemens	TDA4814,4816	x					x			x
Siemens	TDA4817	x					x			x
Toko	TK84812	x			x	x			x	
Toko	TK84819	x		x	x	x			x	
Unitrode	UC3852	x					x			x
Unitrode	UC3854	x			x				x	
Unitrode	UC3855 A/B	x			x				x	

List of Available Integrated Circuits

Table 1 above shows a reasonably comprehensive list of power factor correction integrated circuit manufacturers, the chips they make, and the characteristics of these chips. Each manufacturer differentiates itself by supplying a different set of features, simplifying either the chip design or the external circuitry. Please refer to individual data sheets that are available from the various manufacturers for specifics on the particular combination of features and benefits of a particular chip.

Typical Block Diagrams of Average and Peak Boost PFC

Figures 7 and 8 are simplified block diagrams of the two principal boost converter topologies. They show the signal flows clearly. Average current control (similar to voltage mode control) has an extra operational amplifier to control the current. Peak current control (similar to current mode control) compares the peak switch current to a rectified sine-wave reference signal and terminates the switch current when it equals the reference.

Average current boost PFC

Figure 7 shows a typical average current boost power factor correction circuit.
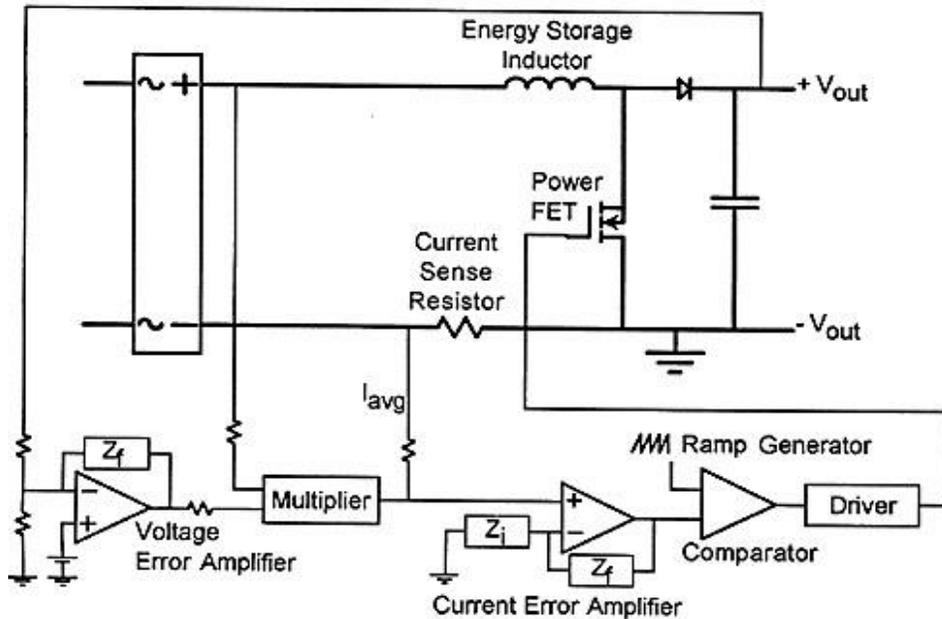
Figure 7. Block diagram of typical average current PFC circuit

The input AC waveform is rectified to produce a half-sine-wave voltage with a peak value of about 160 volts on 120-volt mains or 320 volts on 240-volt mains. There is very little capacitive filtering directly across the rectified line input. Any current, which flows from the input, flows through the energy storage inductor and returns through the current sense resistor. When the power FET turns on, energy is stored in the inductor, and when the power FET turns off, at least some of this energy is delivered to the output filter capacitor and load (not shown) through the diode. With boost converters, the output voltage must be higher than the maximum input voltage. Typical output voltage is 380 to 400 volts DC This output voltage is divided down and compared to a reference in the voltage error amplifier. This is the slow loop, and it needs to have a bandwidth in the range of 10 to 12 Hz. The output of this error amplifier is fed to one input of a multiplier and is used to scale the value of the other input of the multiplier, which is a current proportional to the half-sine-wave rectified input voltage. The output of the multiplier is a signal (usually a current) with a half-sine-wave rectified shape and amplitude proportional to the output of the voltage error amplifier. This signal is compared to the input current by summing the multiplier output with a current proportional to input current at the positive input of the current error amplifier. The other (negative) input of the current error amplifier is grounded through a resistor, and the current feedback loop acts to keep the positive input at ground potential (zero volts). The output of the current error amplifier is compared to a ramp and used to generate a pulse-width-modulated drive signal for the power FET.

Peak Current Boost PFC

Figure 8 shows a typical peak (current mode) power factor correction circuit. As before, the input from the AC mains is rectified to produce a half-sine-wave rectified voltage that varies from zero to about 360 volts, depending on the AC mains voltage. With peak current boost PFC, the average current is not important and the current sense resistor is typically placed in series with the source terminal of the power FET. As before, the output voltage must be

greater than the maximum input voltage, and is typically 380 to 400 volts DC This voltage is sensed with a divider string and compared to a reference in the voltage error amplifier. As before, this is the slow loop and should have a bandwidth between 10 and 12 Hz. Like the average current circuit, the half-sine-wave rectified AC input voltage is fed to one input of a multiplier and the voltage error amplifier output is fed to the other, so that the multiplier output is again a half-sine-wave rectified waveform scaled in amplitude by the output of the voltage rror amplifier.

At this point, operation of the two circuits differs. The power FET current is compared to the half-sine-wave rectified reference signal, and when it equals this signal the power FET is turned off.

Figure 8. Block diagram of typical peak current (current mode) PFC circuit

The power FET remains off until it is turned on again by a fixed-frequency clock, which is part of the PFC control chip. A compensating ramp usually derived from the clock oscillator (ramp and clock not shown in the diagram) is either subtracted from the reference signal or added to the current signal to provide open loop stability of the current mode control circuit when the duty cycle exceeds 50% as it does at low input voltage. This type of regulation, current mode control, does not lend itself to testing. The best way to test for stability of the current loop is to inject a current in parallel with the multiplier output and then to measure the transconductance from control voltage (output of the multiplier) to controlled output (current in the energy storage inductor). In order to do this, the operating point must be frozen (as explained later in this paper), and the test results compared to plots like those given in Figures 4 and 5 earlier in this paper.

Specific Examples of Average and Peak PFC Circuits

Figures 9 and 12 are specific examples of average and peak power factor correction circuits. There are variations from manufacturer to manufacturer in the specific implementations of the circuits required. There are also differences in features. The two examples chosen demonstrate the many choices that are available from the various vendors.

Average Current PFC Circuit, the Linear Technology LT1249

Figure 9 is a simplified block diagram of the LT1249 power factor correction IC, redrawn from the schematic furnished in the Linear Technology data sheet. The block diagram also shows injection points for feedback loop testing.
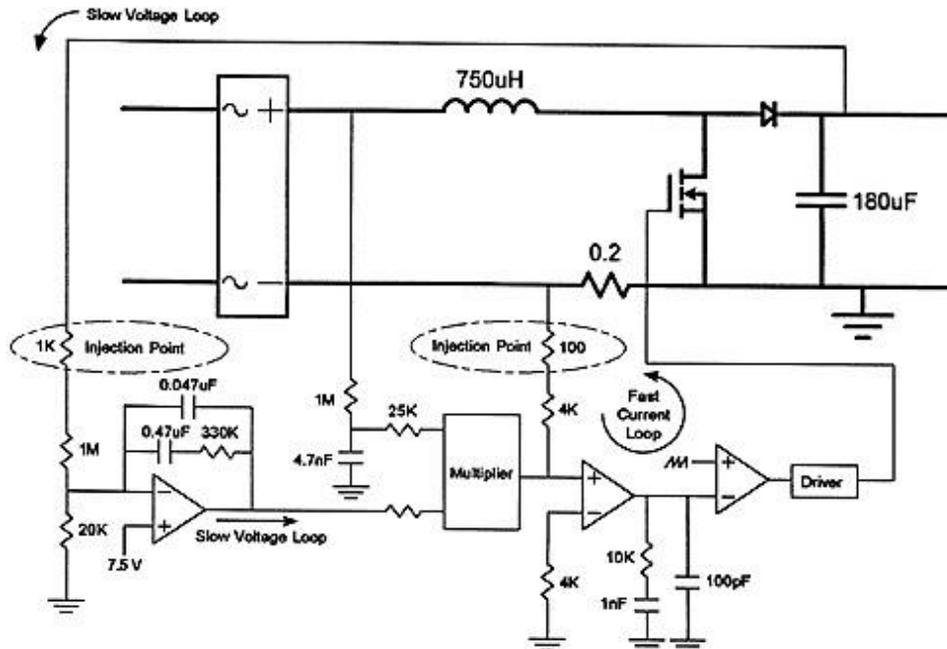
Figure 9. LT1249 Average Current PFC Integrated Circuit

The voltage control loop, "slow voltage loop" in this example, senses the output voltage with a resistive divider and compares the result to a 7.5-volt reference. The nominal output voltage in this case will be 382.5 volts. Provision is made for a zero and pole in the amplifier transfer function to adjust the loop phase margin. The ideal bandwidth for this loop is 10 to 12 Hz, and the phase margin should be between 50 and 70 degrees. The problem for the designer, which he or she will probably pass on to the user, is that the actual loop performance depends on the multiplier parameters and these are not specified in the data sheet. For this particular part, only a typical value of multiplier output current is given, with no min or max value. That is why it is essential to test the feedback loop, at least on a sample basis if not on every production unit. If you are a purchaser or user of power supplies with PFC incorporated in the design, ask for data on the loops periodically (not just on the qualification unit). This data should come in the form of a Bode plot, which is a plot of gain and phase versusfrequency, clearly showing the bandwidth and phase margin.

Operation and Testing of the Current Feedback Loop (fast loop)

The other feedback loop in the LT1249 is the fast loop that senses the input current and controls it to make it match the shape of the input voltage. This loop should have a bandwidth of at least 3 kHz, again with phase margin of 50 to 70 degrees. This loop must be tested also since the loop gain is dependent on the transconductance of the internal error amplifier and the transconductance varies almost 4:1 according to the data sheet. The reference for this loop is the multiplier output current, which has the shape of a rectified sine wave and an amplitude controlled by the output of the voltage error amplifier (slow loop). Current flowing through the 0.2-ohm current sense resistor creates a voltage, which causes current to flow upward in the 4K input resistor to the fast current loop error amplifier. In this case, the reference current from the multiplier and the current from the controlled variable (input current) through the 4K resistor sum at the positive input of the current error amplifier. The negative input of the error amplifier is grounded through another 4K resistor, so any difference from zero volts at the positive input is amplified and forms a reference voltage for the PWM comparator. A fixed amplitude, fixed-frequency ramp is applied to the other input of the comparator, and the points where the ramp crosses the DC level from the error amplifier output set the switching points and thereby duty cycle of the power FET.

The problem with this fast current loop is that the dynamic operating point is constantly changing. When a frequency response analyzer is used to measure loop gain in a conventional way, the resulting Bode plot is actually an average of all the Bode plots from very low current to the peak current. The loop can and sometimes does oscillate either at very low or very high current, while showing stabilityon an average basis.

The solution to this problem is to "freeze" the operating point of the current loop. This "freezing" requires setting DC values for the input and output voltages and for the output of the voltage error amplifier so that the operating point of the circuit represents actual conditions for some instantaneous point of time. The instantaneous input voltage is given by

$$Ein = Vrms * sqrt(2) * sin(theta)$$

where Ein is the test DC input voltage, Vrms is the rms value of input voltage if AC voltage were being used in the test, and is the equivalent input sine wave phase angle for the operating point being tested. The instantaneous input current Iin for a given input power level Pin is given by the equation

$$Iin = (Pin / Vrms) * sqrt(2) * sin(theta)$$

where Iin is the DC input current and the other terms are as previously defined. The output voltage is set by connecting the output of the PFC circuit to an adjustable shunt regulator. The final step in "freezing" the operating point is to disable the voltage error amplifier (typically by shorting the negative input to ground) and then using a DC power supply with a resistive load if necessary to supply the voltage normally supplied by the error amplifier output. This voltage is used to set the DC input current Iin to the value calculated in the previous equation. Figure 10 shows the simplified block diagram with these changes implemented so the current loop can be tested.
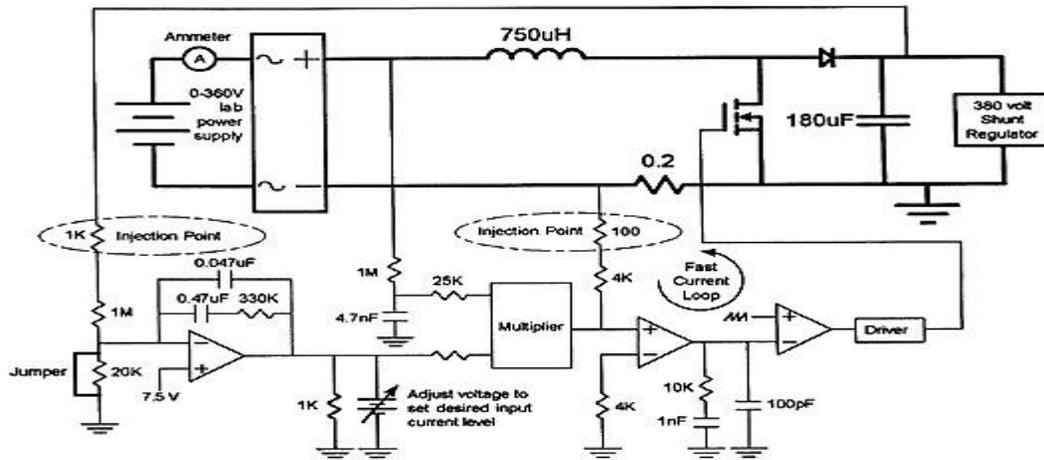
Figure 10. Average current mode PFC modified to test current loop

The technique for testing the stability, bandwidth, phase margin, and gain margin is given in detail in reference 2, but a simplified version is as follows:

Figure 11 is a block diagram of a test setup for making loop measurements. Care has to be taken in choosing test equipment since the voltages involved are near 400 volts. For the voltage loop, the injection transformer is connected across the 1K resistor in series with the 1M resistor and the frequency is swept from at least 1 Hz to 100 Hz. The voltage on each side of the injection resistor is measured and recorded at each measurement frequency, and the ratio of output voltage (across the 180 µF capacitor) to the input voltage (voltage at the junction of the 1K injection resistor and the 1M resistor) is plotted versus frequency to form a Bode plot. The bandwidth is the frequency at which the gain is unity (zero dB), the phase margin is the phase reading when the gain is unity and the gain margin is gain (in dB) when the phase reading is zero. The goal is 10 to 12 Hz bandwidth with 50 to 70 degrees of phase margin.
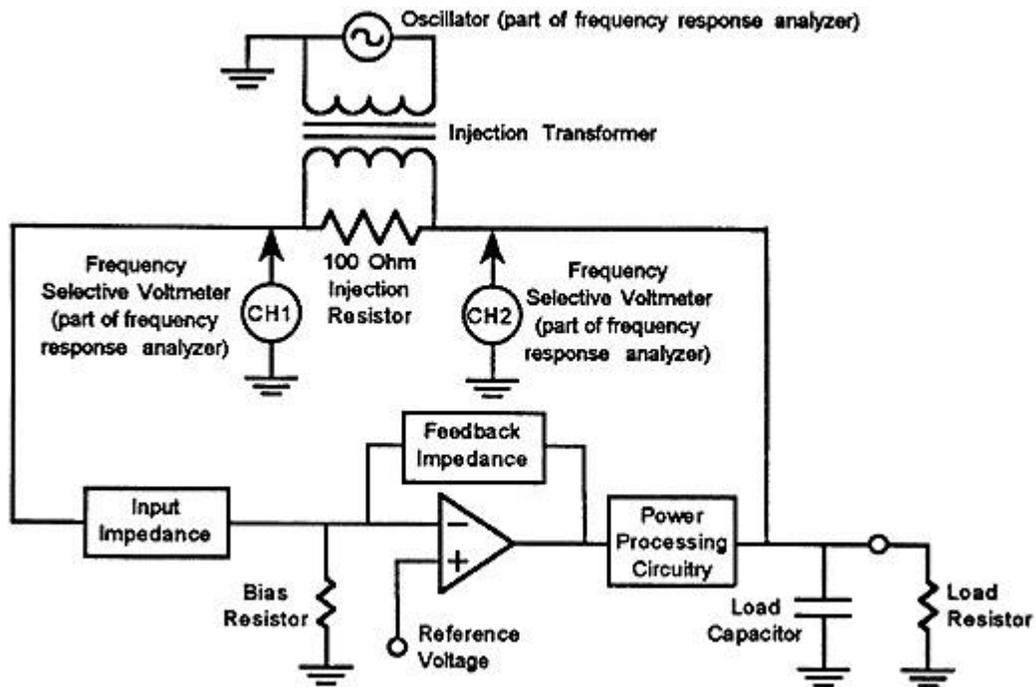
Figure 11. Test setup for measuring open loop transfer function.

The current loop is measured by first "freezing" the operating point as described earlier, then connecting the injection transformer across the 100 ohm injection resistor in series with the 4K input resistor to the error amplifier of the fast current loop. As before, the loop gain is measured as the ratio of the output (junction of the 100 ohm injection resistor and the 0.2 ohm current sense resistor) to the input (junction of the 100 ohm injection resistor and the 4K input resistor). This loop needs to be fast, with a bandwidth of at least 3 kHz, since the reference is quickly changing and the controlled output (input current) must track this reference signal with minimal phase delay. As usual, 50 to 70 degrees of phase margin is an ideal tradeoff between maximizing response time and minimizing overshoot and ringing. Measurement should be made at several operating points.

Peak Current PFC Circuit, the Micro Linear ML4812

Figure 12 shows a simplified block diagram of the Micro Linear ML4812 power factor correction circuit with signal injection points and techniques shown also. The current regulation portion of this chip operates in current mode. As with the other chip, the output voltage is divided down, compared to a reference in an error amplifier, and the output of this error amplifier is used in a multiplier to scale the half-sine-wave rectified signal from the input voltage. The output of the multiplier is a half-sine-wave rectified signal, which is applied to one input of a comparator. The other input of the comparator is a voltage proportional to the instantaneous current in the power FET.
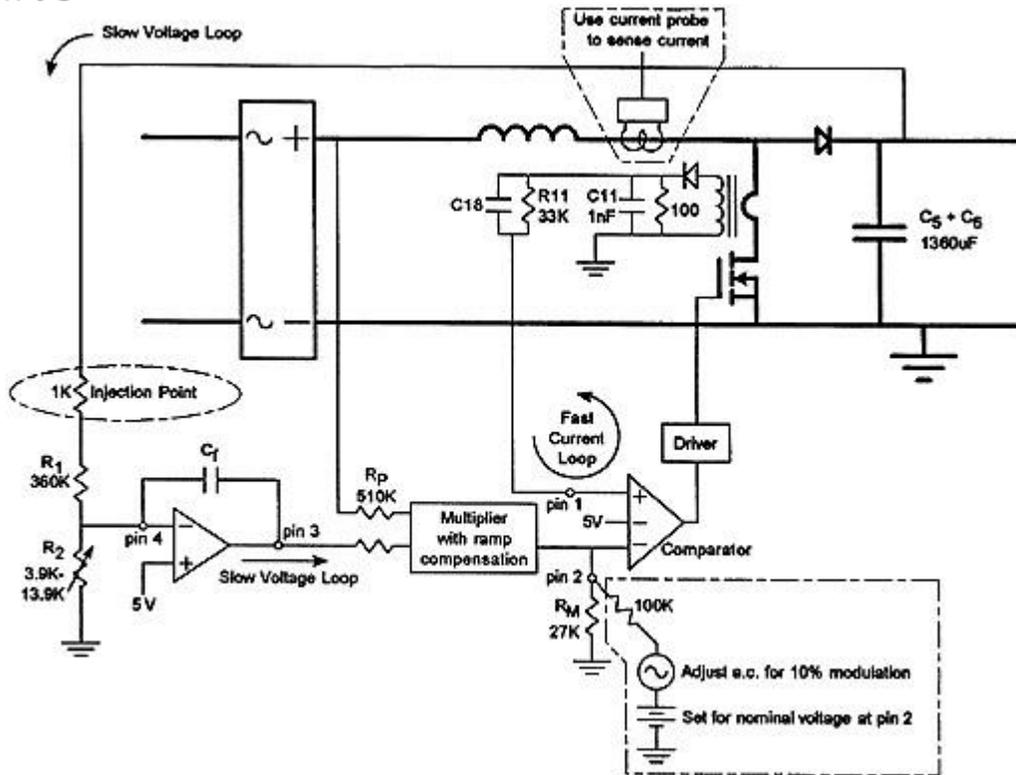
Figure 12. Simplified block diagram of Micro Linear ML4812 PFC circuit

The comparator output controls the power FET, turning it off when the peak current reaches the reference level. The power FET is turned on again by a fixed-frequency clock in the chip. As with all current mode circuits operated above 50% duty cycle, a compensating ramp is required to make the digital current loop stable, and provision for this ramp is provided in the chip.

The voltage loop is tested exactly like it is in the average current chip described above. In this case, the injection resistor is in series with a 360K resistor connected to the 380-volt output. The requirements for this voltage loop are the same, 10 to 12 Hz bandwidth and 50 to 70 degrees of phase margin.

The current loop cannot be tested directly. It can be easily tested indirectly, however. Instead of creating a sinusoidal error voltage in series with the feedback loop as was done in all the previous measurements, a parallel injection scheme is used to disturb the operating point of the loop. The transfer function is then measured from the signal injection point to the controlled variable, in this case, input current. The measurement that results is the closed loop transfer function, the transfer function from reference to output. As before, the operating point has to be "frozen" in exactly the same way in order to do a meaningful measure of current loop stability. Rather than a direct measurement of bandwidth and phase margin, the closed loop transfer function is flat out to about the bandwidth of the open loop transfer function, then starts to roll off. The amount of peaking at the frequency where the rolloff starts is related to the phase margin of the feedback loop. By making the closed loop measurements and comparing the results to the sample plots shown in Section 2, accurate assessment of the stability margins can be made. Closed loop data can also be converted to open loop data to see the actual open loop Bode plots. The alternative, described to us recently by a leading power supply manufacturer, is "to follow the circuits in the manufacturer's data sheets and pray a lot."

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